REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested. Claims 19-46 are pending in the present application.

Claims 42-46 were rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the written description requirement. More specifically, the Official Action states that the "claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention." However, this rejection is respectfully traversed because the subject matter in Claims 42-46 is respectfully submitted to be supported in the original specification for at least the following reasons.

Initially, the undersigned notes that in the previous rejection, this ground included claims 39-41, which portion of the rejection was withdrawn based on the support pointed out in the Amendment filed on October 26, 2009. The undersigned appreciates the progress made on this point. However despite the support provided in that response for claims 42-46, these claims still remain rejected as allegedly failing to find support in the originally filed specification based on two specific claim elements which are called into question. Accordingly additional support for these two claim elements is identified below.

First, the phrase "wherein said state engine includes a plurality of state elements which comprise a plurality of local shared memories which provides a composite bandwidth that is a sum of all bandwidths associated with each one of the plurality of local shared memories" is objected to in claim 42. To assist the Examiner in understanding the basis for this language in the original specification, the following table breaks this language down into its component parts and maps each part to the originally filed specification. It will be appreciated that such mappings provided herein are intended to be exemplary rather than exhaustive.

Claim Language	**Original Specification**
"State Engine"	Page 9, line 28 – Page 10, line 22
"Plurality of State Elements"	Page 8, lines 20 – 26 (defines single state element; Page 8, lines 30-32 ("In the State Cell each field of the record is stored as a single state variable in its own State Element. These State Elements are then chained together in a pipeline", i.e., a plurality of State Elements.
"Which Comprise A Plurality of Local Shared Memories"	Page 15, original claims 14 and 15, "each said state element comprises local memory"; Page 14, original claim 1, "state element means providing coherent parallel access to shared state". Page 5, lines 31-32, "State elements are the key components which perform serialization of accesses into a shared memory."
"Composite Bandwidth Is the Sum of all Bandwidths Associated with each One of the Plurality of Local Shared Memories"	Page 9, lines 18-19 "Increasing the total state storage by multiplying State Cells can also increase overall state access bandwidth".

By breaking down the objected to claim language, and exemplary support therefore, it is the hope of the undersigned that, if the Examiner continues to believe that there is some lack of written descriptive support for this claim pursuant to 35 U.S.C. § 112, first paragraph, then the Examiner is kindly requested to further identify the specific word or words in this clause which remain allegedly unsupported so that clarifying word choice amendments can be considered.

Secondly, with respect to claim 46, the Official Action objects to the phrase "a plurality of state engines, wherein one or more of said state engines are applied to a system bus and wherein said one or more of said state engines operate separately from each other." Again, to further the prosecution on this point, the undersigned provides a table breaking down this objected to language and illustrating examples of descriptive support in the originally filed specification.

Claim Language	**Original Specification**
"A Plurality of State Engines"	Page 5, line 32, "The state elements are combined in state engines..."
"Wherein One or More of Said State Engines are Applied to A System Bus"	Page 5, line 32, "The state elements are combined in state engines and connected to a bus." Also see Figure 2.
"Wherein said one or more of said state engines operate separately from each other."	Page 9, lines 33-34, "The state engine may issue (private) system commands to the state arrays", i.e., independent of other state engines.

As with claim 42, the undersigned would greatly appreciate it if the Examiner would consider this information and then indicate which, if any, of the particular sub-elements

of the objected to claim language are still believed to pose a problem. Moreover, if this lack of written descriptive support rejection remains the sole point of contention upon evaluation of the comments below relating to the art rejection, the undersigned further urges the Examiner to contact the undersigned telephonically so that this ground of rejection can be resolved expeditiously and the entire application be passed to issuance.

For at least the above reasons, reconsideration and withdrawal of the rejection of claims 42-46 under 35 U.S.C. §112, first paragraph, are respectfully requested.

Claims 19-40 were rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Steely, Jr. et al. (U.S. Patent No. 6,088,771, herein "Steely") in view of Dieffenderfer et al. (U.S. Patent No. 5,822,608, herein "Dieffenderfer") and Wang et al. (US Patent Publication No. 2002/0062415).

Briefly recapitulating, independent Claim 19 is directed to a state engine that receives multiple requests from a parallel processor for a shared state. The state engine includes at least one state element means, the at least one state element means adapted to operate, atomically, on the shared state in response to a request made by the parallel processor. The request includes at least a command directing the at least one state element means on how to perform an operation on the shared state. The operation includes reading, modifying, and writing back said shared state. The state engine also includes a memory connected to the at least one state element means and configured to store the shared state.

The claimed at least one state element unit advantageously achieves, for example, faster access for the parallel processor to the shared state, as shown for example in Figure 5(b) of the present application and its corresponding description in the specification.

Turning to the applied art, Steely discloses a technique that reduces a latency of a memory barrier operation used to impose an inter-reference order between sets of memory reference operations issued by a processor to a multiprocessor system having a shared memory. More specifically, Figure 2 shows a local switch 200 communicating with a plurality of processors P1 to P4 such that inputs from the processors are serialized before being sent to a shared memory 150. Figure 2 shows that the switch 200 includes an arbiter 240 that arbitrates, among input queues from the processors P1 to P4, to grant access to the Arb bus 170, where the requests are ordered into a memory reference request stream. The arbiter 240 selects the request stored in the input queues for access to the bus in accordance with an arbitration policy, such as a conventional round-robin algorithm, as disclosed in Steely in the paragraph bridging columns 6 and 7.

Thus, the device of Steely does not teach or suggest that a request from any of the processors P1 to P4 includes at least a command directing the arbiter 240 regarding how to perform an operation (i.e., reading, modifying, and writing back said shared state) on the shared memory 150, as recited, among other things, by the independent claims.

In other words, the arbitration system of Steely does not perform an operation on the shared memory 150 based on a command from the processors P1 to P4 but rather acts based on the round-robin algorithm, which is not provided by the processors P1 to P4. Steely simply queues and arbitrates updates to memory from the processors and does not teach or suggest processors sending commands to the state engine directing it regarding how to update the memory.

In this regard, if a processor in Steely needs to increment a shared memory location, then the processor needs to read the data from the memory, increment the value, write it back to the memory, and then issue a memory barrier instruction to synchronize this update with all the other processes. However, this operation delays the other processors from accessing that memory location until the first processor has finished the complete sequence read-modify-write operation, as illustrated in Figure 5(b).

To the contrary, the claimed invention avoids this latency because any number of state processors may instruct the state engine via the requests, for example, to increment the same shared state and the processors may immediately continue with other processing. Thus, the processors do not have to wait for the whole operation read-modify-write to be performed, as illustrated by Figure 5(a).

Dieffenderfer is cited solely for the proposition that parallel processors are known and that it would have been obvious to have modified Steely to include such parallel processors. While the undersigned does not necessarily agree with that assessment,

and reserves the right to further contest that issue later, it is not deemed at the moment to be the clearest point regarding why the combination of Steely, Dieffenderfer and Wang do not render the claimed combinations unpatentable.

As correctly recognized by the Official Action, neither Steely nor Dieffenderfer teach or suggest the combination set forth in Applicant's claim 19 combination including the feature of "said operation including reading, modifying, and writing back said shared state." Accordingly, Wang is cited as an alleged teaching of this feature and is used to modify the combination of Steely and Dieffenderfer. The undersigned strenuously disagrees with this aspect of this ground of rejection for at least the following reasons.

Initially, the Examiner will recall the telephone interview on October 23, 2009 in this application in which it was agreed that the claims as proposed to be amended at that time (and as are currently pending) were patentable over the combination of Steely in view of Dieffenderfer and further in view of Tetrick, but that the amendments would not be allowed at that time because further search would be performed. That further search has evidently revealed Wang, which the Examiner now relies on in place of Tetrick in this latest claim rejection.

However, Wang simply teaches a network switch. The Official Action appears to be relying on Wang for the allegation that Wang discloses both Read/Modify/Write (herinafter RMW) and the use of 'shared state'. The undersigned disagrees with this characterization of Wang and respectfully submits that the Official Action incorrectly equates the use of a shared memory with the presence of a shared state. For example,

it does not necessarily follow that, simply because Wang includes a shared memory buffer 104, that Wang also implements a shared state associated with that shared memory. On the contrary, memory may be used as a common storage area with the control of that storage area and the state of that storage area being processed elsewhere. Wang teaches no more than a store and forward facility.

Consider that Wang fails to mention 'state' **anywhere** within its specification. This is hardly surprising because the shared memory is being used simply as storage, either for PDUs (which have been received ahead of their being transmitted by the appropriate port or ports (if multi-cast or broadcast)) or for routing information. The 'state' management of the system is not explicitly taught or described. It is 'maintained' through the arbiter enforcing a data bus arbitration schedule as described in [0052] as:

> "[0052] The data bus arbitration schedule 200 is divided into time frames 202. Each time frame 202 being further subdivided into time slots 204. A deterministic data bus arbitration schedule 200 is enforced. Read, write, and modify memory access cycles are performed during time slots 204. Memory access cycles are assigned to DMA devices 120 and it is left up to each individual DMA device 120 to make use of the assigned time slot(s) 204. This removes the necessity of sending/receiving memory access requests and therefore eliminating the overhead involved in conveying and processing thereof, leading to a more efficient use of the memory bandwidth B."

Also in paragraph [0052] Wang teaches that the necessity of 'sending/receiving memory access requests', which would be employed to query the system's maintained state and issue a response in dependence upon it, have been removed through the use

of a deterministic arbitration schedule. So, rather than teaching a system that 'maintains' a shared state, instead Wang teaches a method whereby time-slots are allocated in a deterministic arbitration schedule, avoiding the need to maintain shared state and to operate based upon that shared state.

This conclusion is further supported in paragraph [0059] of Wang, wherein it is stated that:

> [0059] Shown in the diagram is data switching node 300 having arbiter 308 implementing the memory access scheme presented above with respect to FIG. 2. The arbiter 308 coordinates 326 the access of the DMA devices 120 to the data bus 106 by pacing repeatedly through the access schedule specified via the time frame 202-in a cyclical fashion. The use of a deterministic access schedule greatly simplifies the design of the data switching node 300.

Wang fails to teach queuing or list management. Instead, the disclosure of Wang relies upon providing a deterministic arbitration schedule and allowing the DMA units to operate in dependence of their having a slot in order to complete their outstanding tasks (ie a decentralized, fixed slot, distributed task scheme).

To reiterate, Wang teaches only a system that implements a store-and-forward system, which operates autonomously. It does not maintain a shared state system and the teachings in Wang, when combined with those of Dieffenderfer and Steely, would fail to disclose those of the instant application, at least for that reason since one of ordinary skill in the art would have been unable to generate the claim 19 system which

includes, among other features, "said operation including reading, modifying, and writing back said shared state." Similar comments apply to the remaining independent and dependent claims.

Accordingly, Applicant respectfully submits that the combination of Dieffenderfer with Steely and Wang, as put by the Examiner, would simply not be considered by the person of ordinary skill in the art and, even if they were, that combination would not lead to the conclusion that Applicant's claims are unpatentable over them. Accordingly, reconsideration and withdrawal of the rejections of claims 19-40 under 35 U.S.C. § 103(a) over Steely in view of Dieffenderfer and Wang are respectfully requested.

Claim 41 stands rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Steely, Jr. et al. (U.S. Patent No. 6,088,771, herein "Steely") in view of Dieffenderfer et al. (U.S. Patent No. 5,822,608, herein "Dieffenderfer") and Wang et al. (US Patent Publication No. 2002/0062415), and further in view of Tetrick (U.S. Patent Publication No. 2001/0021967). Claim 41 is dependent from claim 19 and, therefore, is allowable for at least the reasons set forth above with respect thereto since Tetrick fails to remedy the deficiencies of Steely, Dieffenderfer and Wang.

All of the objections and rejections raised in the outstanding Office Action having been addressed, it is respectfully submitted that this application is in condition for allowance and a notice to that effect is earnestly solicited. Should the Examiner have any questions regarding this response or the application in general, she or he is invited to contact the undersigned at (540) 361-1863.

Respectfully submitted,

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